

# Low Power 2-Bit ADC Array with Serial Output, Phase II Project

SBIR/STTR Programs | Space Technology Mission Directorate (STMD)



## ABSTRACT

Microwave interferometers for NASA missions such as PATH employ the GeoSTAR instrument, consisting of 600 receivers. Each receiver requires I and Q ADCs (analog-to-digital converters) for signal digitizing at 1GHz before further processing in the cross-correlators. Power consumption as well as instrument volume and weight are critical in space born instruments. During Phase I, Pacific Microchip Corp. designed the block diagrams and circuits of a monolithic array consisting of sixteen 2-bit ADCs. A serializer is integrated to reduce the number of outputs from 32 to 1. This reduces the power consumption per ADC and resolves the problem of wiring congestion in the interface with cross-correlators. For further power reduction, a novel metastability programming feature is integrated into the ADC latches. The clock distribution is fundamentally simplified as well. The 2-wire serial I2C (Inter-Integrated Circuit) interface allows all 1200 ADCs of the GeoSTAR instrument to be calibrated and optimized. Phase I work provided a complete definition and in silico validation of the monolithic ADC array with serial output. Phase II of the project will produce a fieldable product. In order to facilitate the commercialization efforts in Phase III, a Complementary Metal-Oxide-Semiconductor (CMOS) Silicon-on-Isolator (SOI) technology will be used for fabrication.

## ANTICIPATED BENEFITS

### To NASA funded missions:

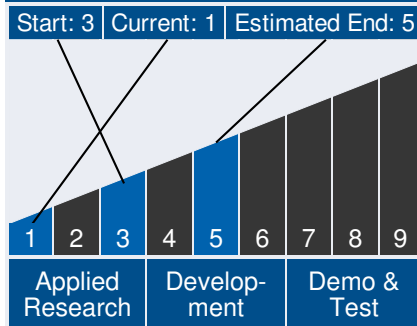
The unique characteristics of the proposed ADC array make it ideal for parallel digitizing applications that require power efficiency at high quantization rate. Oversampling can be used when more than 2-bit resolution is required. Such ADCs are critical components in multichannel wireless communication systems. Advanced ADC arrays are also required for neural implants, image sensors and sensor networks. The ADC array will be implemented using commercial 45nm SOI CMOS



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## Technology Maturity



## Management Team

### Program Executive:

- Richard Leshner

### Program Managers:

- Gary Jahns
- Richard Leshner

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technology offering low device cost and extremely power efficient operation. The proposed Pacific Microchip Corp. Serializers and Deserializers (SerDes) capable of operating at a line rate of up to 32Gb/s are the essential blocks required for the next generation 100Gb/s (4x25Gb/s) Ethernet. We also plan to offer the ADC array as an IP block for integration in Systems On Chip (SoC).

### To the commercial space industry:

The extra-low power ADC arrays with serial outputs featuring power optimization capability depending on the required BER, high quantization frequencies, and convenient control through a two wire interface can be used in radiometer and interferometer instruments such as GeoSTAR. These instruments apply passive and active microwave technologies that are under development by NASA in its mission to provide inexpensive data for many different fields including science, agriculture, geology, weather forecast, climatology, and civil aviation. The potential application of the ADC arrays in space-based wireless communication systems promises to lower the cost of exploration data delivery to users.

### Management Team (cont.)

#### Project Managers:

- Gary Jahns
- Robert Jones

#### Principal Investigators:

- Dalius Baranauskas
- Dalius Baranauskas

### Technology Areas

#### Primary Technology Area:

Science Instruments, Observatories, and Sensor Systems (TA 8)

- └ Remote Sensing Instruments and Sensors (TA 8.1)
  - └ Microwave, Millimeter-, and Submillimeter-Waves (TA 8.1.4)

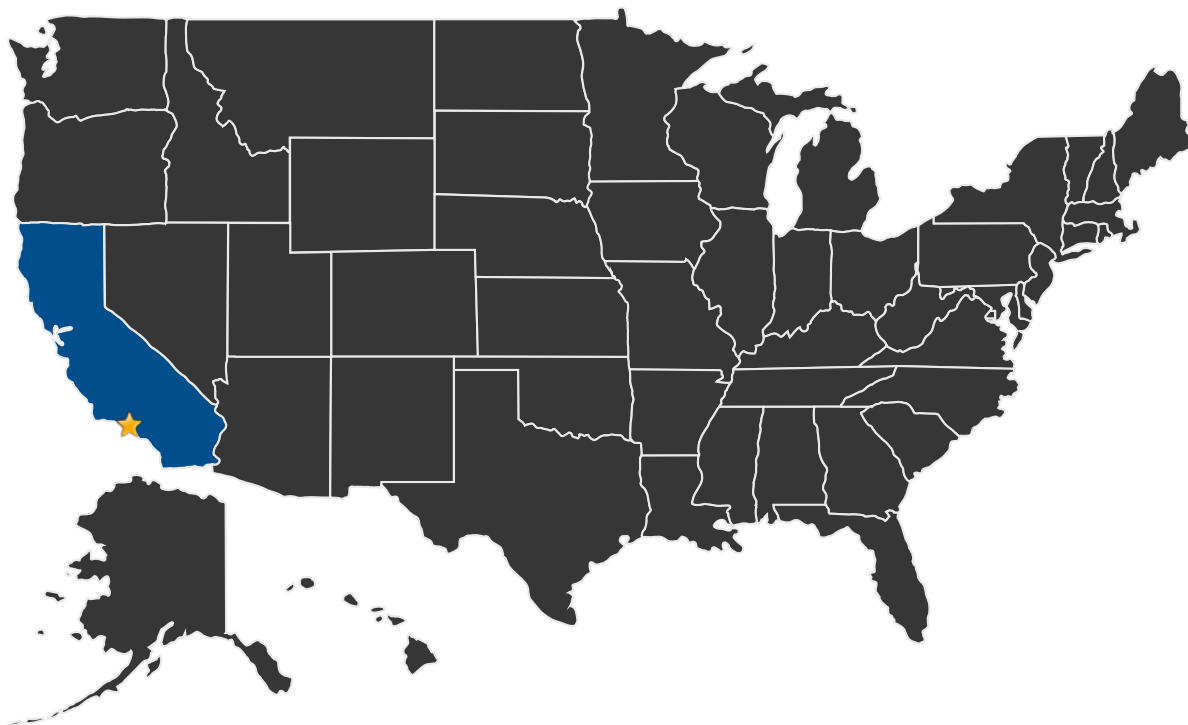
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## U.S. WORK LOCATIONS AND KEY PARTNERS

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■ U.S. States With Work      ★ **Lead Center:**  
Jet Propulsion Laboratory

### Other Organizations Performing Work:

- Pacific Microchip Corporation (Culver City, CA)
- Pacific Microchip Corporation (Culver City, CA)

## PROJECT LIBRARY

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### Presentations

- Final Summary Chart
  - (<https://techport.nasa.gov:443/file/15592>)

Completed Project (2011 - 2013)

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## DETAILS FOR TECHNOLOGY 1

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### Technology Title

Low Power 2-Bit ADC Array with Serial Output