Active Project (2011 - 2019)

High Performance Spaceflight Computing (HPSC) Project

Game Changing Development Program | Space Technology Mission Directorate (STMD)

ANTICIPATED BENEFITS

To NASA funded missions:

The HPSC Formulation Study determined that a rad-hard general-purpose multi-core architecture is the best fit for future NASA application needs. Multi-core provides direct architectural support for power scaling and a range of fault tolerance methods. Furthermore, a multi-core flight computing system can be operated flexibly, with ongoing dynamic trades among computational performance, energy management and fault tolerance. This Game-Changing investment in a next-generation flight computing system will address both performance and system-level advances, and serve to reinvent the role of computing in space.

DETAILED DESCRIPTION

Space-based computing has not kept up with the needs of current and future NASA missions We are developing a next-generation flight computing system that addresses NASA computational performance, energy management and fault tolerance needs, through 2030

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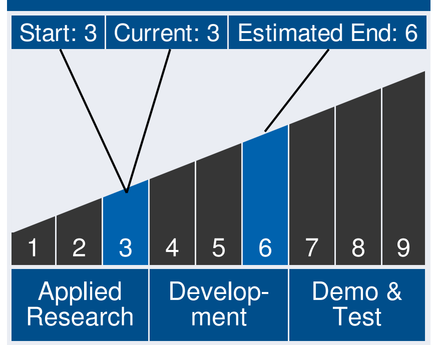
Technology Maturity



Management Team

Program Executive:

- Lanetra Tate

Program Manager:

- Mary Wusk

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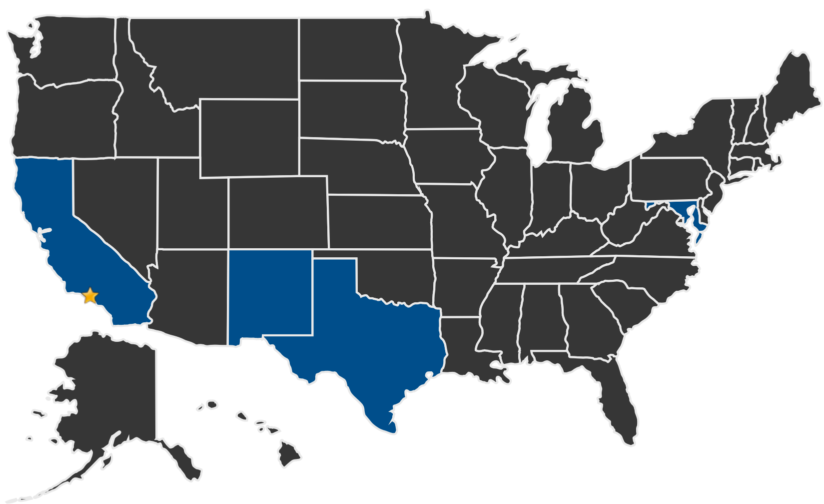
U.S. WORK LOCATIONS AND KEY PARTNERS



U.S. States With Work

Lead Center:
Jet Propulsion Laboratory

Management Team *(cont.)*

Project Manager:

- Richard Doyle

Principal Investigator:

- Stephen Horan

Technology Areas

Primary Technology Area:
Entry, Descent, and Landing Systems (TA 9)
└─ Descent and Targeting (TA 9.2)
  └─ Autonomous Targeting (TA 9.2.8)
    └─ Onboard Dedicated Compute Elements (TA 9.2.8.7)

Modeling, Simulation, Information Technology and Processing (TA 11)
└─ Computing (TA 11.1)
  └─ Flight Computing (TA 11.1.1)
    └─ Radiation-Hardened General Purpose Flight Processor (TA 11.1.1.1)

Secondary Technology Area:
Robotics and Autonomous Systems (TA 4)
└─ Sensing and Perception (TA 4.1)
  └─ Onboard Science Data Analysis (TA 4.1.6)

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Technology Areas *(cont.)*

Additional Technology Areas:

Communications, Navigation, and Orbital Debris Tracking and Characterization Systems (TA 5)

Human Exploration Destination Systems (TA 7)

Science Instruments, Observatories, and Sensor Systems (TA 8)

Entry, Descent, and Landing Systems (TA 9)
- Descent and Targeting (TA 9.2)

Modeling, Simulation, Information Technology and Processing (TA 11)
- Computing (TA 11.1)
  - Flight Computing (TA 11.1.1)
    - Radiation-Hardened General Purpose Flight Processor (TA 11.1.1.1)
    - Radiation-Hardened High-Capacity Memory (TA 11.1.1.2)
    - High Performance Flight Software (TA 11.1.1.3)
    - High Speed Onboard Networks (TA 11.1.1.5)

DETAILS FOR TECHNOLOGY 1

Technology Title

High Performance Spaceflight Computing (HPSC)

Technology Description

This technology is categorized as a hardware component or part for computers

The HPSC Formulation Study identified the range and types of future NASA mission flight applications through the 2030 timeframe. A total of 19 use cases were identified from human spaceflight and robotic science mission scenarios that required significantly higher performance computing than available with current or planned space-qualified computers. The study concluded with a recommendation to pursue an investment for a next-generation flight computer for future NASA missions. Rad-hard general-purpose multicore was identified as the most promising architecture for a future NASA flight computer for the following reasons:

• Rad-hard general-purpose multicore has the best overall fit to application requirements – provides both general purpose and some digital signal processing capability as well as interoperability with specialized coprocessors.

• Rad-hard general-purpose multicore is conducive to power scaling at the level of individual cores or processors, and the power dissipation issues to address appeared to fit within the available investment resource envelope.

• Rad-hard general-purpose multicore is conducive to thread-based fault tolerance—the ability to segregate failed cores from the pool of available cores in support of graceful degradation.

These architectural features together will allow for unprecedented flexibility in flight computing: choosing the operating point dynamically, trading among performance, energy management and fault tolerance needs as the mission unfolds and science, engineering and exploration objectives evolve.

Capabilities Provided

1. Rad-Hard, General-Purpose, Multicore Processor

- 100X performance of RAD750
- <7W power budget, scalable
- Support for a range of fault tolerance methods
- Interoperable with co-processors

2. System Software, Runtime and Development Environments

- OS, Hypervisor, Debugger, C/C++

3. Middleware Layer - Dynamic System Configuration

- Resource Allocator, Power Manager, Fault Tolerance Manager

4. Evaluation board and reference design kit

It has been more than 15 years since the previous flight computing investment at NASA. A next-generation flight computing capability will be a necessary and timely ingredient for future mission success. Partnered with AFRL, we are taking steps toward realizing that vision.

Potential Applications

The HPSC team is engaging with NASA SMD (e.g., Mars Exploration Program) and HEOMD mission customers representing use cases as developed in the HPSC Formulation Phase Study Report. Via the partnership with AFRL, a similar engagement is occurring with SMC for USAF customers. In addition, HPSC team members are engaging with other potential national-level customers and/or programmatic partners (e.g., NRL/USN).

More specifically, preliminary discussions have taken place with the Mars Exploration Program (MEP) towards a possible Mars 2020 technology payload concept to demonstrate Mars-relevant flight capabilities (e.g., fast traverse, autonomous surface science operations) supported by HPSC capability. These discussions could form the basis of a future Technology Demonstration Project co-funded by the Mars Exploration Program.